IN THE CLAIMS 1, 16, 31, 43, 58, 63, 69, 73

1. (Currently Amended) A method of determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the method comprising:

partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets; and

combining the plurality of simulations to form the complete clock net.

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2. (Original) The method as defined in claim 1, wherein partitioning comprises breaking the complete clock net into a plurality of parts approximating rectangular grid coordinates.

3. (Original) The method as defined in claim 1, further comprising breaking at least one of the plurality of local clock nets down into at least one sub-local clock net.

4. (Original) The method as defined in claim 3, further comprising simulating the at least one sub-local clock net prior to simulating the corresponding local clock net.

5. (Original) The method as defined in claim 1, wherein at least two of the plurality of local clock nets are simulated in parallel.

6. (Original) The method as defined in claim 1, wherein simulating each of the plurality of local clock nets comprises:

extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database;

extracting component values of the elements of the local clock net from the microprocessor network database;

simulating the local clock net based on the layout and the component values; and

extracting a load of the local clock net on the global clock net.

7. (Original) The method as defined in claim 6, wherein simulating the local clock net comprises assuming that the clock arrival times from the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net.

8. (Original) The method as defined in claim 1, wherein simulating the global clock net comprises:

extracting the layout of the global clock net from a microprocessor network database;

extracting component values of the elements of the global clock net from the microprocessor network database;

inserting the simulated loads of the plurality of local clock nets; and

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads.

9. (Original) The method as defined in claim 1, further comprising storing the plurality of simulation results in a Clock Data Model.

10. (Original) The method as defined in claim 1, further comprising evaluating the complete clock net to determine whether the results converge.

11. (Original) The method as defined in claim 10, wherein, if the results do not converge, the method further comprises:

assuming that clock arrival times are those calculated for the simulated global clock net;

re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net;

re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets; and

combining the simulations and re-simulations to form the complete clock net.

12. (Original) The method as defined in claim 11, wherein re-simulating at least one of the plurality of local clock nets comprises:

re-simulating the at least one local clock net based on the layout, the component values, and the calculated clock arrival times; and

extracting a load of the at least one local clock net on the global clock net.

13. (Original) The method as defined in claim 12, further comprising re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net.

14. (Original) The method as defined in claim 11, wherein re-simulating the global clock net comprises:

inserting the simulated or re-simulated loads of the plurality of local clock nets; and

re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads.

15. (Original) The method as defined in claim 11, further comprising storing the plurality of simulation and re-simulation results in a Clock Data Model.

16. (Currently Amended) An apparatus for determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the apparatus comprising:

means for partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;

means for simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

means for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets; and

means for combining the plurality of simulations to form the complete clock net.

17. (Original) The apparatus as defined in claim 16, wherein means for partitioning comprises means for breaking the complete clock net into a plurality of parts approximating rectangular grid coordinates.

18. (Original) The apparatus as defined in claim 16, further comprising means for breaking at least one of the plurality of local clock nets down into at least one sub-local clock net.

19. (Original) The apparatus as defined in claim 18, further comprising means for simulating the at least one sub-local clock net prior to simulating the corresponding local clock net.

20. (Original) The apparatus as defined in claim 16, wherein at least two of the plurality of local clock nets are simulated in parallel.

21. (Original) The apparatus as defined in claim 16, wherein means for simulating each of the plurality of local clock nets comprises:

means for extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database;

means for extracting component values of the elements of the local clock net from the microprocessor network database;

means for simulating the local clock net based on the layout and the component values; and

means for extracting a load of the local clock net on the global clock net.

22. (Original) The apparatus as defined in claim 21, wherein means for simulating the local clock net comprises means for assuming that the clock arrival times from the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net.

23. (Original) The apparatus as defined in claim 16, wherein means for simulating the global clock net comprises:

means for extracting the layout of the global clock net from a microprocessor network database;

means for extracting component values of the elements of the global clock net from the microprocessor network database;

means for inserting the simulated loads of the plurality of local clock nets; and

means for simulating the global clock net based on the layout, the component values, and the simulated local clock net loads.

24. (Original) The apparatus as defined in claim 16, further comprising means for storing the plurality of simulation results in a Clock Data Model.

25. (Original) The apparatus as defined in claim 16, further comprising means for evaluating the complete clock net to determine whether the results converge.

26. (Original) The apparatus as defined in claim 25, wherein the apparatus further comprises:

means for assuming that clock arrival times are those calculated for the simulated global clock net;

means for re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net;

means for re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets; and

means for combining the simulations and re-simulations to form the complete clock net.

27. (Original) The apparatus as defined in claim 26, wherein means for re-simulating at least one of the plurality of local clock nets comprises:

means for re-simulating the at least one local clock net based on the layout, the component values, and the calculated clock arrival times; and

means for extracting a load of the at least one local clock net on the global clock net.

28. (Original) The apparatus as defined in claim 27, further comprising means for re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net.

29. (Original) The apparatus as defined in claim 26, wherein means for re-simulating the global clock net comprises:

means for inserting the simulated or re-simulated loads of the plurality of local clock nets; and

means for re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads.

30. (Original) The apparatus as defined in claim 26, further comprising means for storing the plurality of simulation and re-simulation results in a Clock Data Model.

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31. (Currently Amended) An apparatus for determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the apparatus comprising:

a partitioner for horizontally and vertically partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;

at least one local clock net simulator for simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net;

a global clock net simulator for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets; and

a merging unit for combining the plurality of simulations to form the complete clock net.

32. (Original) The apparatus as defined in claim 31, wherein the partitioner comprises a cutter for breaking the complete clock net into a plurality of parts approximating rectangular grid coordinates.

33. (Original) The apparatus as defined in claim 31, wherein the partitioner vertically sub-partitions at least one of the plurality of local clock nets down into at least one sub-local clock net.

34. (Original) The apparatus as defined in claim 33, wherein the at least one local clock net simulator simulates the at least one sub-local clock net prior to simulating the corresponding local clock net.

35. (Original) The apparatus as defined in claim 31, further comprising at least a second local clock net simulator wherein at least a second of the plurality of local clock nets is simulated in parallel with the at least one local clock net.

36. (Original) The apparatus as defined in claim 31, wherein the at least one local clock net simulator comprises:

a layout extractor for extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database;

a component value extractor for extracting component values of the elements of the local clock net from the microprocessor network database;

a local clock net simulator for simulating the local clock net based on the layout and the component values; and

a load extractor for extracting a load of the local clock net on the global clock net.

37. (Original) The apparatus as defined in claim 36, wherein the local clock net simulator assumes for the simulation that the clock arrival times from the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net.

38. (Original) The apparatus as defined in claim 31, wherein the global clock net simulator comprises:

a layout extractor for extracting the layout of the global clock net from a microprocessor network database;

a component extractor for extracting component values of the elements of the global clock net from the microprocessor network database;

a load insertion unit for inserting the simulated loads of the plurality of local clock nets; and

a simulator for simulating the global clock net based on the layout, the component values, and the simulated local clock net loads.

39. (Original) The apparatus as defined in claim 31, further comprising a Clock Data Model for storing the plurality of simulation results.

40. (Original) The apparatus as defined in claim 31, further comprising a convergence evaluator for evaluating the complete clock net to determine whether the results converge.

41. (Original) The apparatus as defined in claim 40, wherein, when the results are found not to converge:

the apparatus assumes that clock arrival times are those calculated for the simulated global clock net;

the at least one local clock net simulator re-simulates at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net;

the global clock net simulator re-simulates the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets; and

the merging unit combines the simulations and re-simulations to form the complete clock net.

42. (Original) The apparatus as defined in claim 41, further comprising a Clock Data Model for storing the plurality of simulation and re-simulation results.

43. (Currently Amended) A computer-readable medium having stored thereon computer-executable instructions for performing a method of determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the method comprising:

partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets; and

combining the plurality of simulations to form the complete clock net.

44. (Original) The computer-readable medium as defined in claim 43, wherein partitioning comprises breaking the complete clock net into a plurality of parts approximating rectangular grid coordinates.

45. (Original) The computer-readable medium as defined in claim 43, wherein the method further comprises breaking at least one of the plurality of local clock nets down into at least one sub-local clock net.

46. (Original) The computer-readable medium as defined in claim 45, wherein the method further comprises simulating the at least one sub-local clock net prior to simulating the corresponding local clock net.

47. (Original) The computer-readable medium as defined in claim 43, wherein at least two of the plurality of local clock nets are simulated in parallel.

48. (Original) The computer-readable medium as defined in claim 43, wherein simulating each of the plurality of local clock nets comprises:

extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database;

extracting component values of the elements of the local clock net from the microprocessor network database;

simulating the local clock net based on the layout and the component values; and

extracting a load of the local clock net on the global clock net.

49. (Original) The computer-readable medium as defined in claim 48, wherein simulating the local clock net comprises assuming that the clock arrival times from the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net.

50. (Original) The computer-readable medium as defined in claim 43, wherein simulating the global clock net comprises:

extracting the layout of the global clock net from a microprocessor network database;

extracting component values of the elements of the global clock net from the microprocessor network database;

inserting the simulated loads of the plurality of local clock nets; and

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads.

51. (Original) The computer-readable medium as defined in claim 43, wherein the method further comprises storing the plurality of simulation results in a Clock Data Model.

52. (Original) The computer-readable medium as defined in claim 43, wherein the method further comprises evaluating the complete clock net to determine whether the results converge.

53. (Original) The computer-readable medium as defined in claim 52, wherein, if the results do not converge, the method further comprises:

assuming that clock arrival times are those calculated for the simulated global clock net;

re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net;

re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets; and

combining the simulations and re-simulations to form the complete clock net.

54. (Original) The computer-readable medium as defined in claim 53, wherein re-simulating at least one of the plurality of local clock nets comprises:

re-simulating the at least one local clock net based on the layout, the component values, and the calculated clock arrival times; and

extracting a load of the at least one local clock net on the global clock net.

55. (Original) The computer-readable medium as defined in claim 54, wherein the method further comprises re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net.

56. (Original) The computer-readable medium as defined in claim 53, wherein re-simulating the global clock net comprises:

inserting the simulated or re-simulated loads of the plurality of local clock nets; and

re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads.

57. (Original) The computer-readable medium as defined in claim 53, wherein the method further comprises storing the plurality of simulation and re-simulation results in a Clock Data Model.

58. (Currently Amended) A method of determining and analyzing clock insertion delays for a microprocessor design having a grid-based clock distribution net, the method comprising:

partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

combining the plurality of simulations to form the complete clock net; and

analyzing the complete clock net to predict the clock skew for a given data transfer path.

59. (Original) The method as defined in claim 58, wherein analyzing comprises:

adjusting an insertion delay of the involved elements of the given data transfer path; and

re-simulating at least one local clock net involved in the given data transfer path.

60. (Original) The method as defined in claim 59, further comprising, when the at least one re-simulated local clock net is connected to at least one sub-local clock net, evaluating the clock arrival times to determine whether the sub-local clock net should be re-simulated.

61. (Original) The method as defined in claim 59, further comprising evaluating the at least one re-simulated local clock net load to determine whether at least one higher clock net connected to the at least one re-simulated local clock net should be re-simulated.

62. (Original) The method as defined in claim 59, further comprising storing the plurality of simulation and re-simulation results in a Clock Data Model.

63. (Currently Amended) An apparatus for determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the apparatus comprising:

means for partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;

means for simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

means for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

means for combining the plurality of simulations to form the complete clock net; and

means for analyzing the complete clock net to predict the clock skew for a given data transfer path.

64. (Original) The apparatus as defined in claim 63, wherein means for analyzing comprises:

means for adjusting an insertion delay of the involved elements of the given data transfer path; and

means for re-simulating at least one local clock net involved in the given data transfer path.

65. (Original) The apparatus as defined in claim 64, further comprising, when the at least one re-simulated local clock net is connected to at least one sub-local clock net, means for evaluating the clock arrival times to determine whether the sub-local clock net should be re-simulated.

66. (Original) The apparatus as defined in claim 64, further comprising means for evaluating the at least one re-simulated local clock net load to determine whether at least one higher clock net connected to the at least one re-simulated local clock net should be re-simulated.

67. (Original) The apparatus as defined in claim 64, further comprising means for storing the plurality of simulation and re-simulation results in a Clock Data Model.

68. (Currently Amended) An apparatus for determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the apparatus comprising:

a partitioner for horizontally and vertically partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;

at least one local clock net simulator for simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net;

a global clock net simulator for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

a merging unit for combining the plurality of simulations to form the complete clock net; and

an analyzer for analyzing the complete clock net to predict the clock skew for a given data transfer path.

69. (Original) The apparatus as defined in claim 68, wherein the analyzer comprises a redesign unit for adjusting an insertion delay of the involved elements of the given data transfer path, wherein the at least one local clock net simulator re-simulates at least one local clock net involved in the given data transfer path.

70. (Original) The apparatus as defined in claim 69, further comprising, when the at least one re-simulated local clock net is connected to at least one sub-local clock net, a clock arrival time evaluator for evaluating the clock arrival times to determine whether the sub-local clock net should be re-simulated.

71. (Original) The apparatus as defined in claim 69, further comprising a load evaluator for evaluating the at least one re-simulated local clock net load to determine whether at least one higher clock net connected to the at least one re-simulated local clock net should be re-simulated.

72. (Original) The apparatus as defined in claim 69, further comprising a Clock Data Model for storing the plurality of simulation and re-simulation results.

73. (Currently Amended) A computer-readable medium having stored thereon computer-executable instructions for performing a method of determining clock insertion delays for a microprocessor design having a grid-based clock distribution net, the method comprising:

partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

combining the plurality of simulations to form the complete clock net; and

analyzing the complete clock net to predict the clock skew for a given data transfer path.

74. (Original) The computer-readable medium as defined in claim 73, wherein analyzing comprises:

adjusting an insertion delay of the involved elements of the given data transfer path; and

re-simulating at least one local clock net involved in the given data transfer path.

75. (Original) The computer-readable medium as defined in claim 74, wherein the method further comprises, when the at least one re-simulated local clock net is connected to at least one sub-local clock net, evaluating the clock arrival times to determine whether the sub-local clock net should be re-simulated.

76. (Original) The computer-readable medium as defined in claim 74, wherein the method further comprises evaluating the at least one re-simulated local clock net load to determine whether at least one higher clock net connected to the at least one re-simulated local clock net should be re-simulated.

77. (Original) The computer-readable medium as defined in claim 74, wherein the method further comprises storing the plurality of simulation and re-simulation results in a Clock Data Model.